A 0.2 μm GaAs MESFET TECHNOLOGY FOR 10 Gb/s DIGITAL AND ANALOG IC's

Yasuro Yamane, Masanobu Ohhata, Hiroyuki Kikuchi, Kazuyoshi Asai, and Yuhki Imai

NTT LSI Laboratories and NTT Electronics Technology
3-1, Morinosato-Wakamiya, Atsugi-shi, Kanagawa Pref., 243-01, Japan

ABSTRACT

A 0.2 μm gate length GaAs IC technology is reported. This technology enables the fabrication of both digital and analog IC's using the same process. A 10 Gb/s decision circuit with a 130 mV sensitivity and 215 degree phase margin, and an amplifier with a 20 dB gain and 13 GHz bandwidth were successfully fabricated using this unified process technology.

INTRODUCTION

Ever since the potential of the GaAs MESFET IC for high speeds was shown by T.Mizutani et al (1) in 1979, GaAs IC process technologies have developed rapidly. The basic outline for the GaAs MESFET fabrication process for integrated circuits was suggested by N.Yokoyama et al (2) and K.Yamasaki et al (3,4). This outline is based on selective ion implantation in bulk GaAs wafers for active layer formation and self-aligned n^+-layer formation adjacent to the gate metal for source resistance reduction. Within this framework, gate length shortening and active layer thinning has been tried to improve FET performance.

At this time, the sub-micron gate (0.5 ~ 0.8 μm) GaAs MESFET is under active development for IC applications. One of the main targets of GaAs IC development is the high-speed digital communication system. A 5 Gb/s D-F/F (5) with a 0.8 μm gate FET, an 8 Gb/s D-F/F (6) with a 0.6 μm gate FET, and using a 0.5 μm gate FET, a 5 Gb/s 4-bit shift register (7), a 12 Gb/s 2-bit MUX/DMUX (8), and a 10 Gb/s D-F/F (9) are important achievements of the past several years in this field.

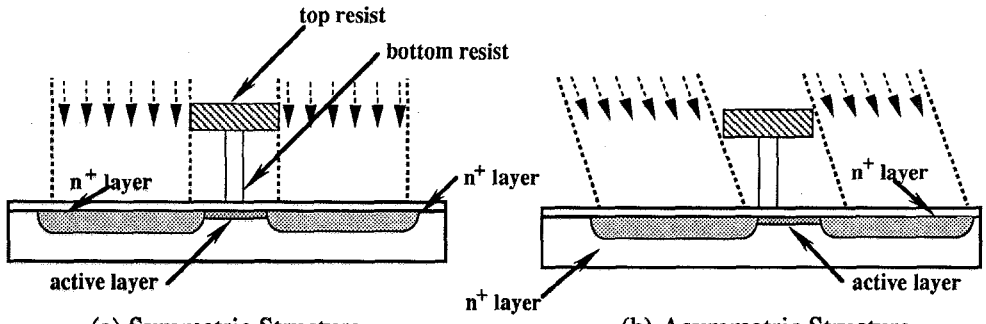
This paper will describe an ultra high-speed 0.2 μm gate length GaAs IC process technology. This technology has made possible 10 Gb/s digital IC's (10-12) and 10 GHz bandwidth analog IC's (13,14) from almost the same process by integrating 40 ~ 50 GHz cut-off frequency FET's. As benchmarks for the applicability of this technology to both digital and analog IC's, this paper will describe an SCFL ring oscillator having a 13.2 ps average delay with a standard deviation of just 0.8 ps, a 10 Gb/s decision circuit with a 130 mV sensitivity and 215 degree phase margin, and an amplifier with a 20 dB gain and 13 GHz bandwidth.

A FET STRUCTURE MODIFICATION FOR DIGITAL AND ANALOG IC APPLICATIONS

This technology (15-18) has two important features. The first is that both the symmetric device structure for digital IC's and the asymmetric structure for analog IC's can be attained simultaneously within the same technology by changing only the n^+ ion implantation angle. The merits of this process compatibility are not just process simplicity but also the potential for mixed analog-digital integrated applications. The second feature is that the 0.2 μm gate length is easily realized using conventional optical photo-lithography and the tri-level resist technique, which is superior to other methods such as EB-lithography from a production standpoint. Patterning finer than the photo-lithographic optical resolution limit is possible only by the SAINT process.

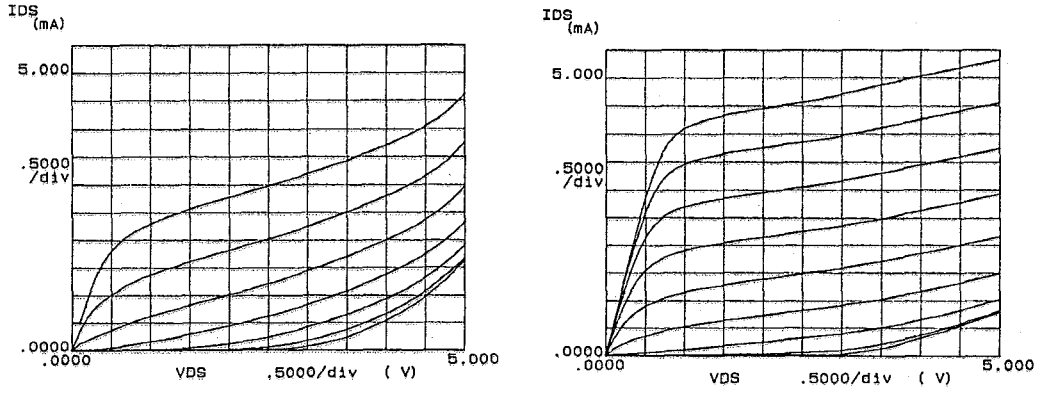
The key to this process technology is shown in Fig. 1. A more detailed description is presented in Refs. 15 and 16. Figure 1 shows the relation of the gate metal and the n^+ layer. The width of the bottom of the T-shaped resist corresponds to the gate metal length, and the top width to the n^+ layer spacing.

CH2870-4/91/0000-0513$01.00 © 1991 IEEE



(a) Symmetric Structure (b) Asymmetric Structure

Figure 1. Symmetric FET Structure for Digital IC's and Asymmetric Structure for Analog IC's



(a) Symmetric E-FET (b) Asymmetric D-FET

(Vg = - 0.6 ~ 0.6 V step 0.2V) (Vg = -1.0 ~ 0.6 V step 0.2V)

Figure 2. I-V Characteristics of Symmetric and Asymmetric FET's

Table 1. Typical Performance of Symmetric and Asymmetric Structure

PARAMETERS	SYMMETRIC	ASYMMETRIC
GATE LENGTH (μm)	0.2	0.2
Vth (mV)	0	-800
f_T (GHz)	50	40
fmax (GHz)	60	70
gm (mS/mm)	400	400
gd (mS/mm)	50	25
Vbreak(gd) (V)	3.5	4.0

Figure 1 (a) is the symmetric structure for digital IC's. Figure 1 (b) is the asymmetric structure for analog IC's. The difference is only the ion implantation angle of the n^+ layer. The spacing between the source-side n^+ layer and gate is shorter than the gate-drain spacing for analog MESFET's, while the same as the latter for digital FET's. The merits of the asymmetric structure are a lower gd and a higher f_{max} and drain-gate breakdown voltage, as shown in Fig. 2 and Table 1. The merits of the symmetric structure are a higher f_T and g_m, and a simpler pattern layout. Because of the relative pattern layout complexity, it is time-consuming to use asymmetric devices in digital IC's. Further information on the correlation between device characteristics and structure will be discussed in the full paper.

THE 0.2μm GaAs MESFET IN CIRCUIT APPLICATIONS

As a demonstration of the feasibility of the 0.2 μm gate length technology, the propagation delay time distribution in a 3-inch wafer is shown in Fig. 3. The delay time was measured through SCFL 19-stage ring oscillators with 40 μm gate-width FET's. Measurement conditions were Vss = -2.5 V and Vcs = 0.6V, which produce the standard bias condition. An average delay time of 13.2 ps with a 0.8 ps standard deviation was found from measuring 24 ring oscillators over a 3 inch wafer. The average power dissipation was 65 mW/gate.

As an example of a digital circuit application (10-12), a decision circuit block diagram and its I/O waveforms at 10 Gb/s are shown in Fig. 4. This circuit has a data input buffer, a 3-stage SCFL differential amplifier, a master slave D-FF, source followers, and an output buffer. The source followers were inserted to reduce the FF output load. Operating at 10 Gb/s with an error rate of less than $1x10^{-10}$, the sensitivity was 130 mV and the phase margin 215 degrees at 10 Gb/s operation. The transit time of the output signal was below 35 ps (20 % ~ 80 %). The total power dissipation was 1.6 W.

As an example of an analog circuit application, the circuit diagram and frequency response of a 13 GHz amplifier are shown in Fig. 5. The circuit configuration is a directly-coupled 2-stage common source circuit with an output-matching source follower and a feedback resistor connected to the input terminal. A gain of 20 dB and bandwidth of 13 GHz was achieved.

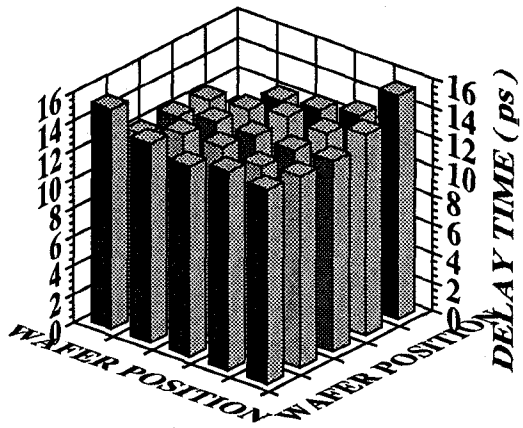
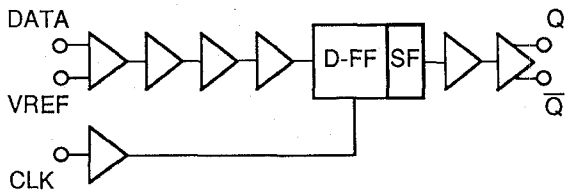


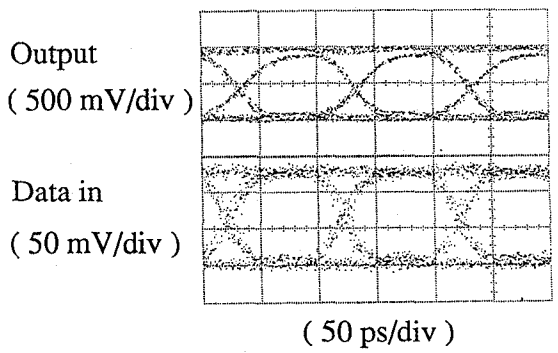
Figure 3.

Propagation Delay Time Distribution of SCFL Ring Oscillators in a 3-inch Wafer



D-FF D-Type Flip Flop
SF Source Follower

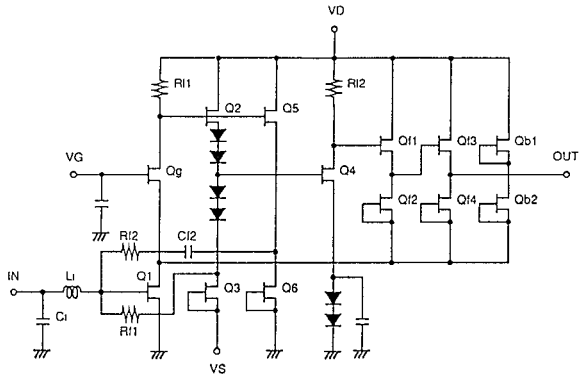
(a) Decision Circuit Block Diagram



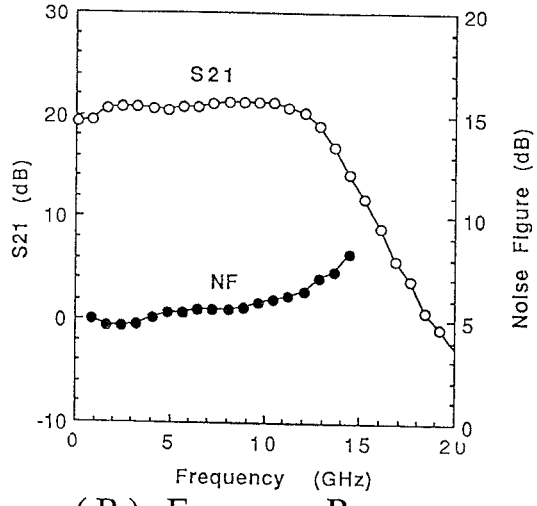
(b) Operating Wave Form at 10Gb/s

Figure 4.

A 10 Gb/s Decision Circuit using 0.2 μm Symmetric FET's



(A) Circuit Diagram



(B) Frequency Response

Figure 5.
A 13 GHz Band Width 18 dB Gain Amplifier using 0.2 μm Asymmetric FET's

CONCLUSION

A 0.2 μm gate length GaAs MESFET process technology that realizes ultra high performance digital and analog IC's has been described. The reliability of these FET's has already been examined (19). The high uniformity of the ring oscillator propagation delay times augurs high yields. Thus it can be said that yield and reliability are well established for 10 Gb/s IC applications.

References

(1) T.Mizutani, M.Ida, and M.Ohmori, "An 80 ps Normally Off GaAs MESFET Logic," Digest of IEEE/MTT-S First Specialty Conference on Gigabit Logic for Microwave Systems, pp.93-101, 1979.

(2) N.Yokoyama, T.Mimura, M.Fukuta, and H.Ishikawa, "A Self-aligned Source / Drain Planar Devices for Ultrahigh-Speed GaAs MESFET VLSIs," 1981 International Solid-State Circuit Conference, pp.218-219, 1981.

(3) K.Yamasaki, K.Asai, T.Mizutani, and K.Kurumada, "Self-Aligned Implantation for n^+ layer Technology (SAINT) for High-Speed GaAs ICs," Electron. Lett., vol. 18, no. 3, pp. 119-121, 1982.

(4) K.Yamasaki, N.Kato, Y.Matsuoka, and K.Ohwada, "EB-Writing N^+ Self-aligned GaAs MESFETs for High-Speed LSIs," IEDM Tech.Dig., pp.166-169, 1982.

(5) Y.Hosono,Y.Kurasima Y.Mima, S.Ichikawa, K.Ueda, H.Hirayama, K.Uetake, T.Furutsuka, and H.Kohzu, "A 5 Gb/s GaAs Monolithic Master -Slave D-type Flip Flop IC," GaAs IC Symp. Tech. Dig. pp 205-208, 1987.

(6) H.Hamano, I.Amemiya, Y.Ihara, H.Onodera, T.Onodera, and S.Shimizu, "8 Gbit/s GaAs logic ICs for Optical Fibre Communication Systems," Electron. lett., vol. 24, no.24, pp.1522-1523, 1988.

(7) K.Ishida, T.Matsunaga, S.Miyano, A.Kameyama, and N.Toyoda, "A 5 Gb/s 4 Bit Shift Resister with 0.5μm WNx-gate GaAs MESFETs," The 20th Conference on Solid State Device and Materials Dig., pp.129-132, 1988.

(8) K.Ishida H.Wakimoto, K.Yoshihara, M.Konno, S.Shimizu, N.Uchitomi, and N.Toyoda, "12 Gb/s GaAs 2-bit Multiplexer / Demultiplexer Chip Set for the SONET STS-192 System," GaAs IC Symp.Tech. Dig., pp.317-320 1989.

(9) M.Shikata, K.Tanaka, K.Inokuchi, Y.Sano, and M.Akiyama, "An Ultra-High Speed GaAs DCFL Flip-Flop MCFF (Memory Cell type Flip Flop)," GaAs IC Symp. Tech. Dig., pp.27-30 1988.

(10) M.Ohhata, Y.Yamane, T.Enoki, S.Sugitani, N.Kato, and M.Hirayama,. "11 Gbit/s Multiplexer and Demultiplexer using 0.15μm GaAs MESFETs," Electron. Lett., vol.26, no.7, pp.467-468, 1990.

(11) M.Togashi, M.Ohhata, K.Murata, H.Kindoh, M.Ino, M.Suzuki, and Y.Yamane, "10 Gb/s GaAs MESFET IC's for Ultra High-Speed Transmission Systems", GaAs IC Symp. Tech. Dig., pp.49-52, 1990.

(12) M.Ohhata, Y.Yamane, T.Enoki, S.Sugitani, N.Kato, K.Hagimoto, and M.Hirayama, "13 Gb/s D-type Flip-Flop IC using GaAs MESFETs," Electron. Lett., vol.26, no.14, pp.1039-1040, 1990.

(13) S.Fujita, Y.Imai, Y.Yamane, and H.Fushimi, "DC - 10 GHz Mixer and Amplifier GaAs ICs for Coherent Optical Heterodyne Receiver," ISSCC Dig. of Tech. Papers, pp.122-123, 1991.

(14) E.Sano, N.Ishihara, H.Kikuchi, and Y.Yamane, "A 10 Gb/s GaAs MESFET Equalizer IC Module," 1991 Symposium on VLSI circuits, to be presented.

(15) K.Yamasaki, K.Asai, and K.Kurumada, "GaAs LSI Directed MESFET's with Self-Alined Implantation for N^+ layer Technology (SAINT)," IEEE Trans. Electron Devices, vol. ED-29, no.11, pp.1772-1777, 1982.

(16) T.Enoki, K.Yamasaki, K.Osafune, and K.Ohwada, "Advanced GaAs SAINT FET Fabrication Technology and its Application to above 9 GHz Frequency Divider," The 17th Conference on Solid State Devices and Materials Dig., pp.413-416, 1985.

(17) T.Enoki, K.Yamasaki, K.Osafune, and K.Ohwada, "0.3 μm Advanced SAINT FET's having Asymmetric N^+-layer for Ultra-High-Frequency GaAs MMIC's," IEEE Trans Electron Devices, vol.ED-35, no.1, pp.18-24, 1988.

(18) Y.Yamane, T.Enoki, S.Sugitani, and M.Hirayama, "5.9 ps/gate Operation with 0.1 μm Gate-Length GaAs MESFET's," IEDM Tech. Dig., pp.894-896, 1988.

(19) J.Nagano, K.Ogawa, H.Sugawara, and M.Hirayama, "Reliability Evaluation of GaAs MESFETs and ICs," Proceedings of the international symposium for testing and failure analysis 89, pp.329-334, 1989.